QUENTIN PIERCE

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Senior Hardware Design Engineer

I am a senior hardware engineer known for automation solutions using skills from both HW and SW domains.

- I use static-code-checking SW to find bugs and improve user's structural design.
- I design automated HW devices and SW tools that push work onto computers.

Technology Background

Design

Discrete analog circuit design theory
Digital circuit and system design theory
HW Validation
FPGA programming and synthesis
Schematics capture and layout CAD SW
Debug using oscilloscopes and logic analyzers
Collaborate with QA for robust code
Designs using TI MSP430 processor
Balances HW/SW trade-offs

Software Engineering

Owned API-gasket SW layers
Owned automation and rules for static-checks
C++, C#, Linux, Perl, PHP

General

FTC Key Volunteer, Led a Makers' Movement
PC repair, PC architecture knowledge, Linux
Technical and instruction writing
Innate intellectual curiosity for technology growth

Professional Experience

Intel Corporation **July 2019-Current**
Software Engineering Contractor
Refactoring a C++ Bus Functional Model and its supporting SW. Updating the documentation concerning the BFM's usage and development practices.

Blue Pearl Software **2017-July 2019**
Software Engineer
Writing lint rules for a commercial Verilog/VHDL static-code checker in OOP C++. Owning key algorithms in the SW's core engine. Writing unit tests in Google's mock test harness.

Part Time Consultant to Imperium-Electronics + Sabbatical **Mar 2017-Current**
Joined the Imperium-Electronics startup as a part-time consultant; providing firmware, schematics, and the board layout for their next product. Spent the year traveling and learning the following:

- Using Texas Instrument's MSP430 processor and programming environment to build a device.
- Using OOP C#, Microsoft Visual Studio, and client-server programming in order to automate the small tasks of some hobbies and of testing the device.

Intel Corporation **2010-2016**

Software Engineer with a central SW tools group

Provided maintenance and new features for custom SW layer between two vendors' software. Wrote rules for automating register-RTL generation. Wrote rules for RTL static checking (linting). Created test automation for static checking flows.

- Reduced RTL model runtime by days using modified checkpointing-SW; co-authored a peer-reviewed paper and disseminated the process and paper to design teams.
- Wrote static-check rules that encapsulated RTL knowledge from senior engineers and passed that knowledge to junior engineers, enabling their quicker learning and faster debugging.
- Led Makers' Movement group inside Intel; resulting in skill development for participants. Learned both teaching skills and IoT design by creating series of after work lectures on IoT, on Linux, node.JS, and on Intel's small form factor computers.

Intel Corporation **2008-2010**

Graduate Level Intern with a CPU validation team

Learned, summarized, and published a process for data capture with Logic Analyzer. Trained fellow engineers in that process. Helped post-silicon validate CPU design. Designed test board using FPGA to drive a proprietary bus. Learned Python and wrote a simple validation tool.

Tektronix Incorporated **2000-2007**

Hardware Design Engineer in the Oscilloscope Product Line

Designed digital interface-circuitry for several Tektronix oscilloscope models. Supported manufacturing by providing troubleshooting processes, design notes, and circuit theory summaries. Designed FPGA firmware and assisted in driver software development. Used oscilloscopes, logic analyzers, and computer-aided test systems.

- Learned Verilog, wrote the firmware, and synthesized FPGA that provided key timing signals to signal acquisition.
- Collaborated with software engineers to develop and debug hardware drivers. Worked with mechanical engineers to update them on trends in computer design.
- Designed two thermal printer systems and learned mechanical control, mixed signal design, and power supply design.
- Designed differential signaling to connect circuit systems together. Used LVDS in two FPGA designs. Designed with modern single-ended signals as well.
- Working knowledge of high-speed analog-to-digital conversion and signal theory.
- Created two interface board designs and documented them for platform reuse.
- Wrote peer-reviewed design specifications, shared them with peers and technicians, and was responsible for training both personnel to become familiar with interface circuitry.

Education

M.S.E.E. from Portland State University

Digital Signal Processing (DSP)	Formal Verification
Device Physics	Advanced Computer Architecture
Post Silicon Electrical Validation	C#

B.S.E.E. from the University of Washington

Major: Analog circuit design	Minor: Digital circuit design